

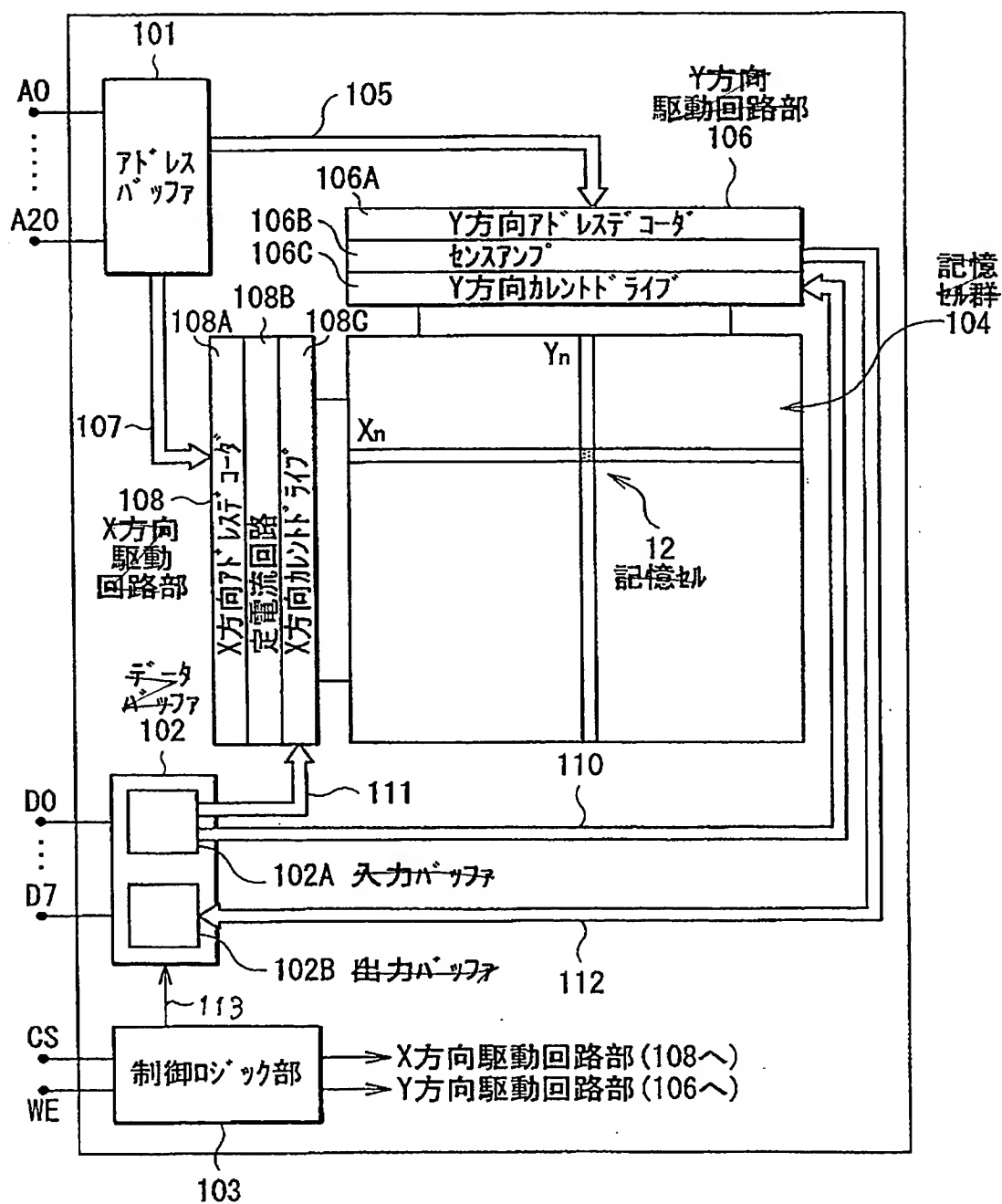
	[FIG. 1]	
	101	ADDRESS BUFFER
	102	DATA BUFFER
	102A	INPUT BUFFER
5	102B	OUTPUT BUFFER
	103	CONTROL LOGIC PORTION
		X-DIRECTION DRIVE CIRCUIT PORTION (TO 108)
		Y-DIRECTION DRIVE CIRCUIT PORTION (TO 106)
	104	MEMORY CELL GROUP
10	12	MEMORY CELL
	106	Y-DIRECTION DRIVE CIRCUIT PORTION
	106A	Y-DIRECTION ADDRESS DECODER
	106B	SENSE AMPLIFIER
	106C	Y-DIRECTION CURRENT DRIVE
15	108	X-DIRECTION DRIVE CIRCUIT PORTION
	108A	X-DIRECTION ADDRESS DECODER
	108B	CONSTANT CURRENT CIRCUIT
	108C	X-DIRECTION CURRENT DRIVE
	[FIG. 2]	
20	80n+1	BIT-DIRECTION UNIT READING CIRCUIT
	102B	OUTPUT BUFFER
	[FIG. 3]	
	102B	OUTPUT BUFFER
	[FIG. 8]	
25	6a	WRITE BIT LINE
	6b	WRITE WORD LINE
	[FIG. 20]	
		SENSING CURRENT VALUE (SELECTED SCALE)
		BIT DECODE VOLTAGE (STANDARDIZED VALUE)
30	[FIG. 21]	
		SENSING CURRENT VALUE (SELECTED SCALE)
		BIT DECODE VOLTAGE (STANDARDIZED VALUE)
	[FIG. 22]	
		VOLTAGE AT SENSING POINT
35		RESISTANCE OF MAGNETORESISTANCE ELEMENT: R_{TMR1} (Ω)
	[FIG. 24]	
		VOLTAGE AT SENSING POINT
		VARIATION OF MR RATIO IN MAGNETORESISTANCE ELEMENT

【書類名】 図面

【図 1】

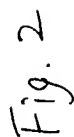
Fig. 1

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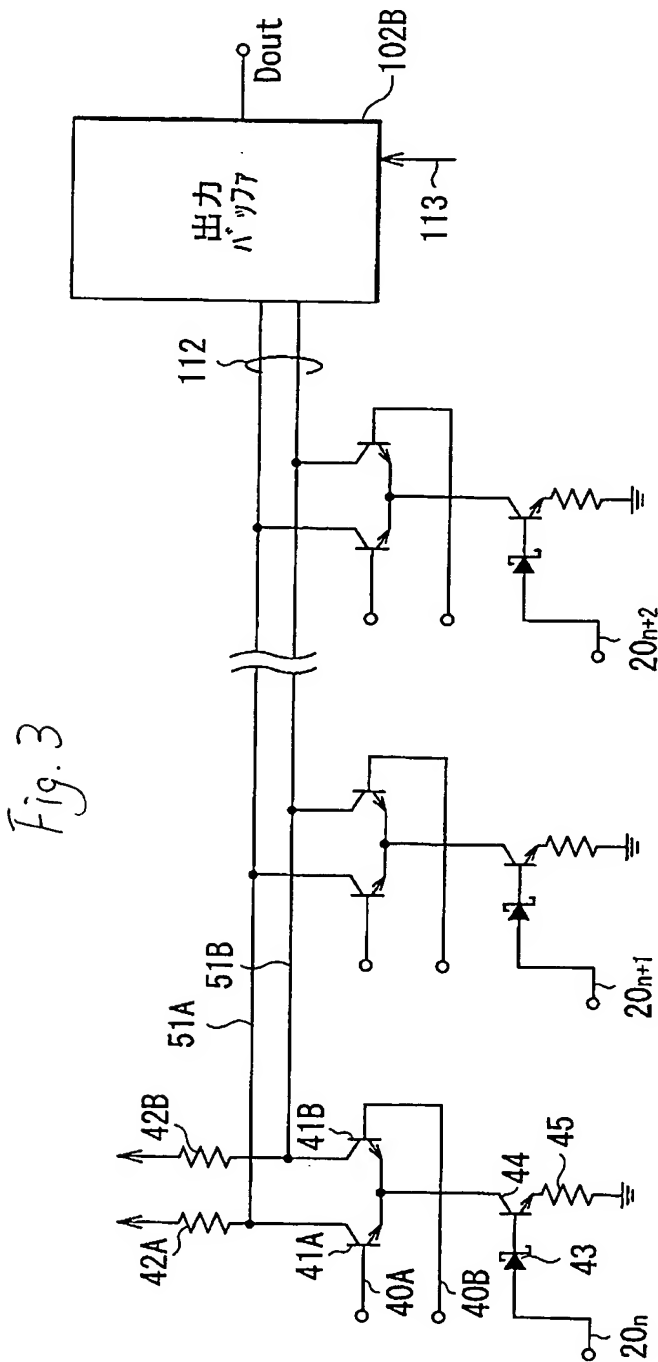
【図 2】

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【図 3】

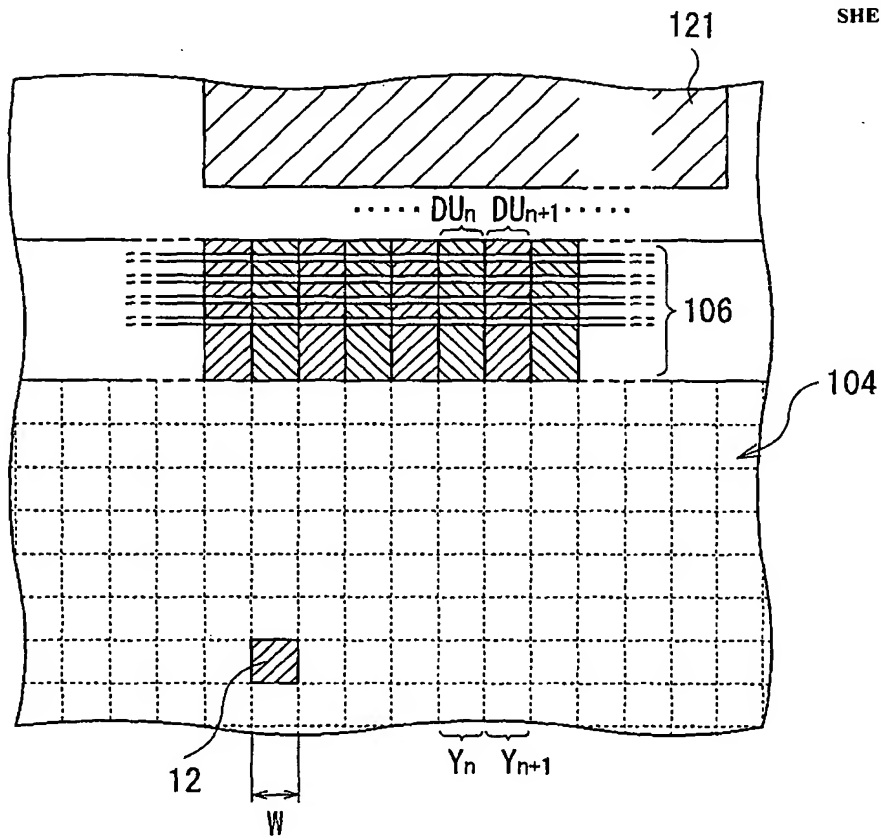
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【図4】

Fig. 4

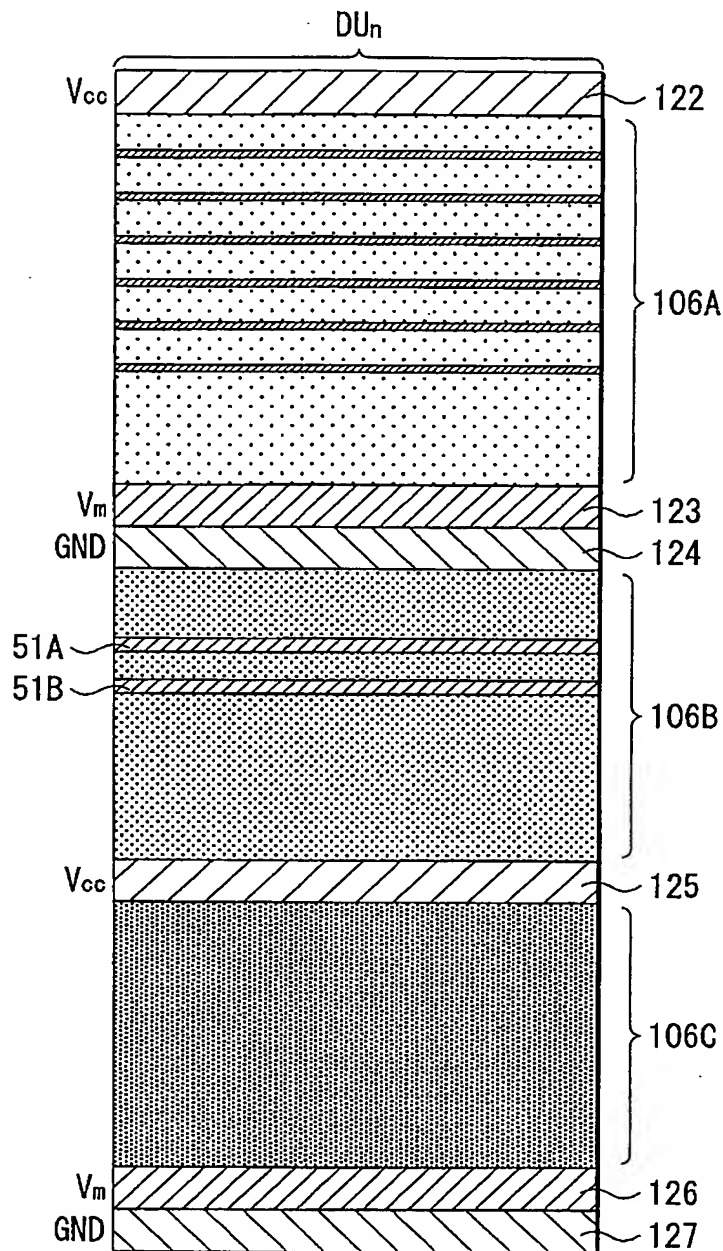
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【図 5】

Fig. 5

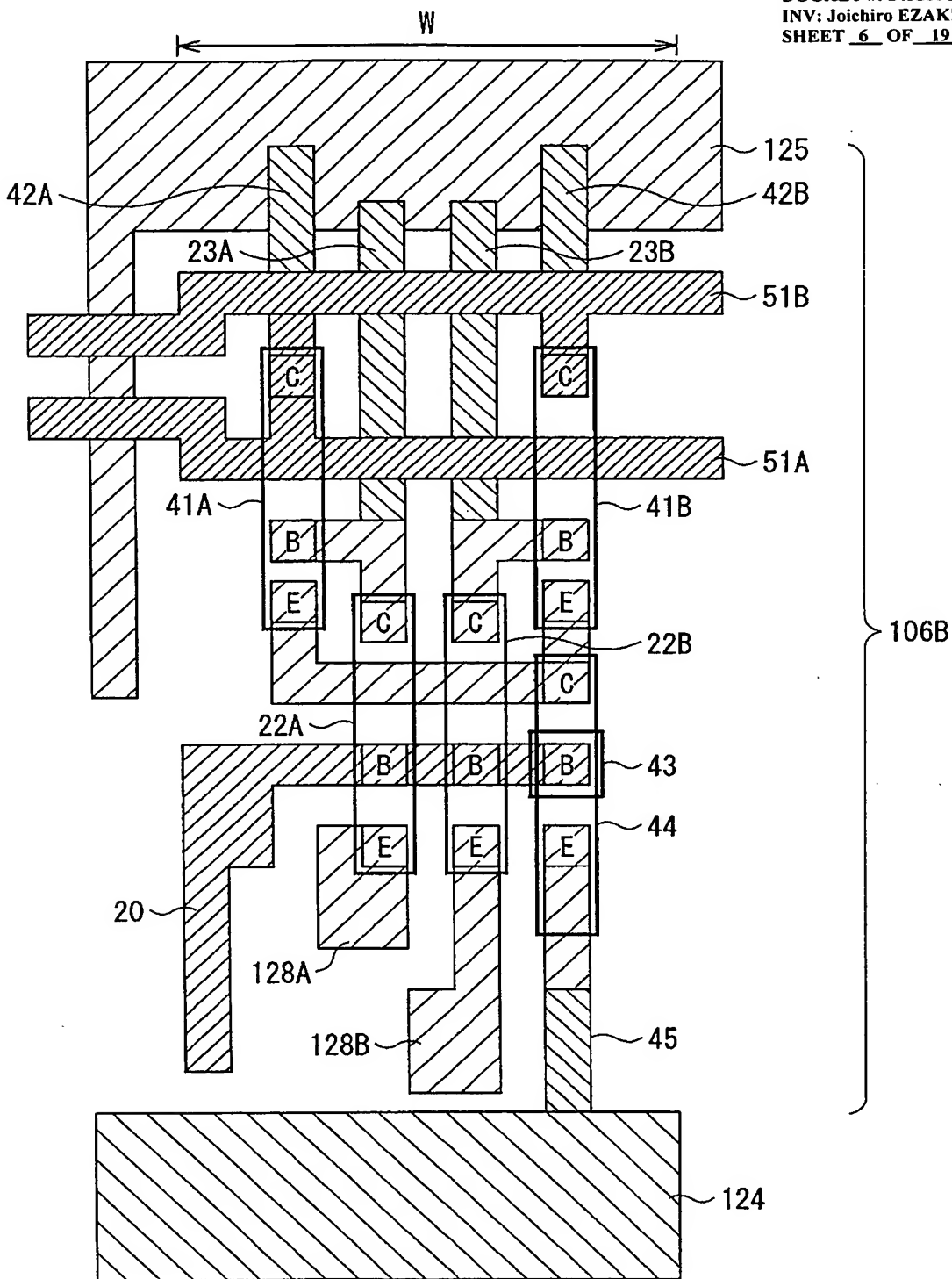
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【図 6】

Fig. 6

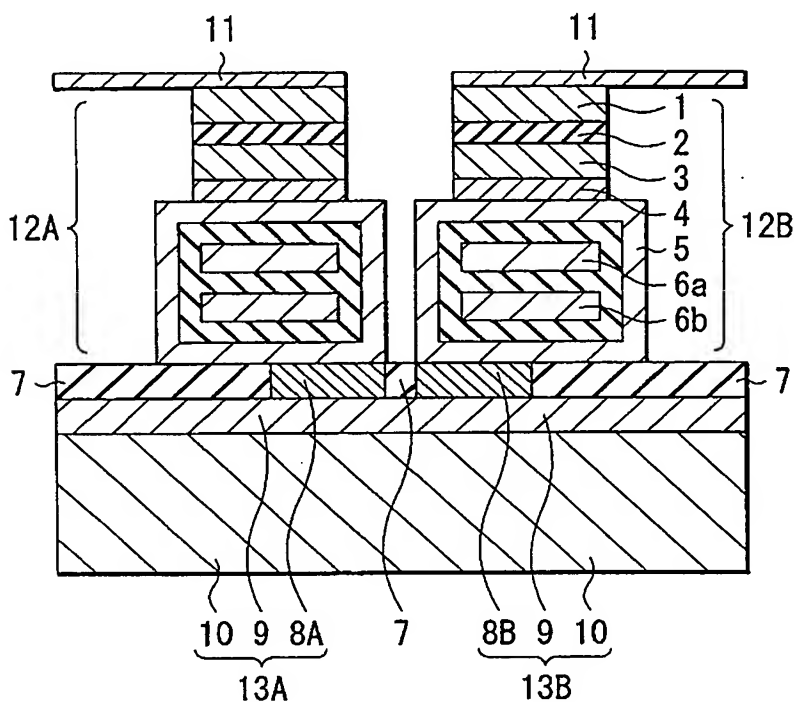
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【図 7】

Fig. 7

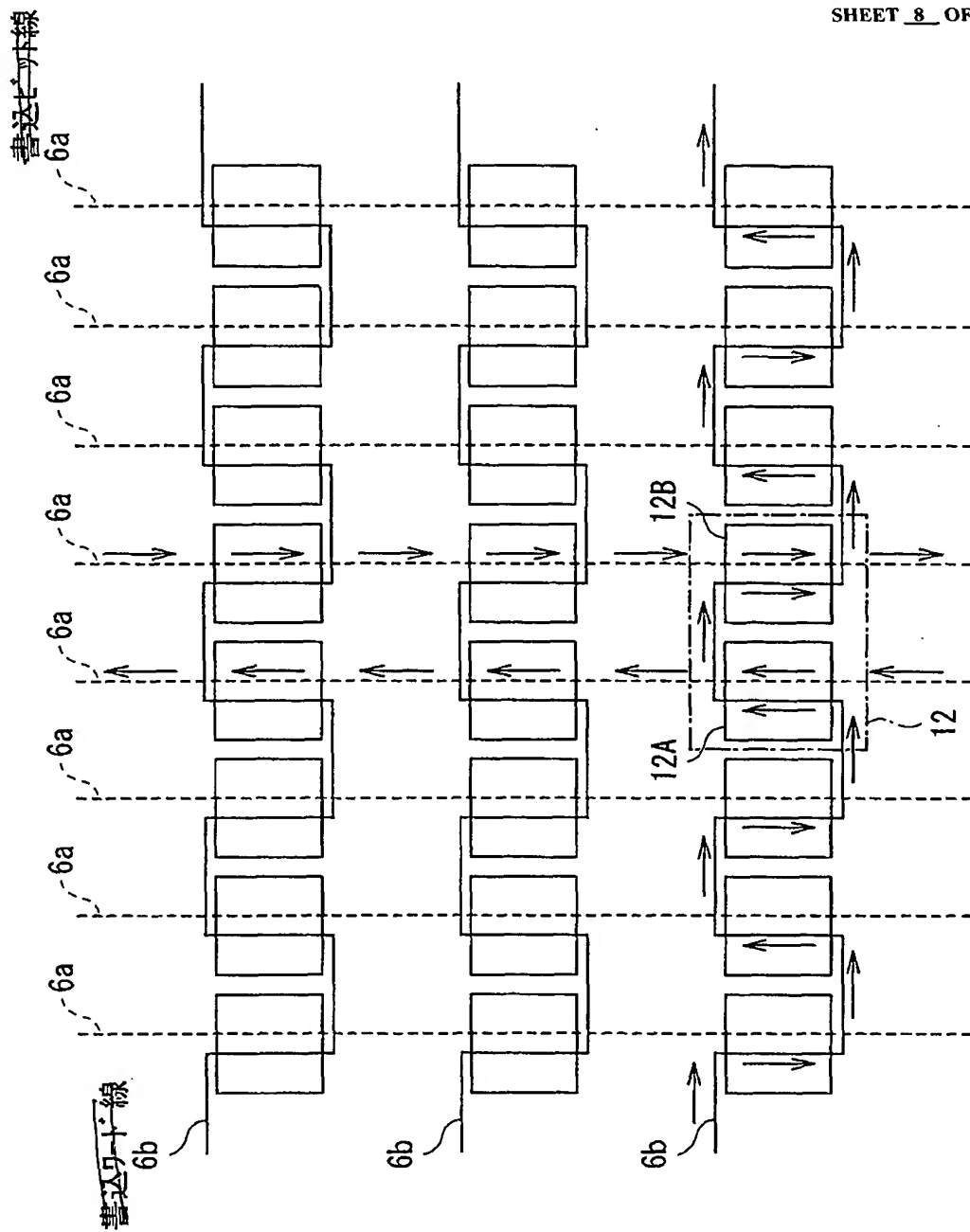
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【図 8】

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Fig. 8



【図 9】

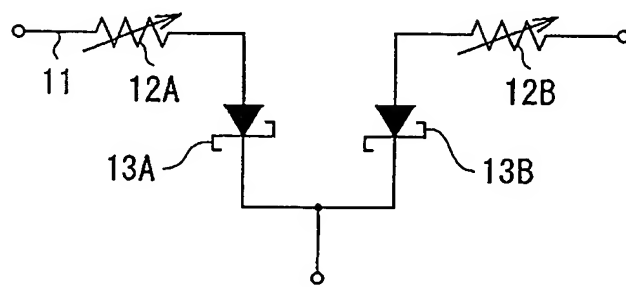
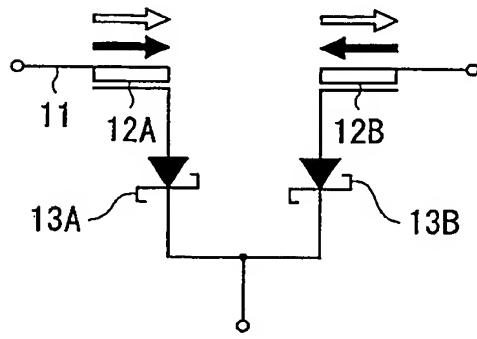


Fig. 9

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【図 10】

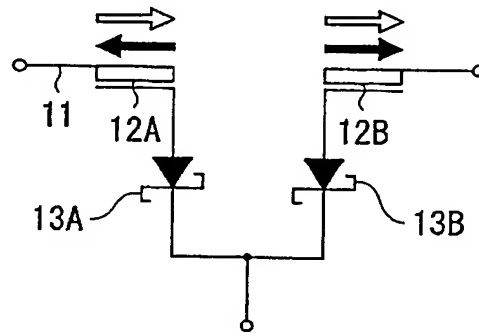
Fig. 10A



「0」

(A)

Fig. 10B



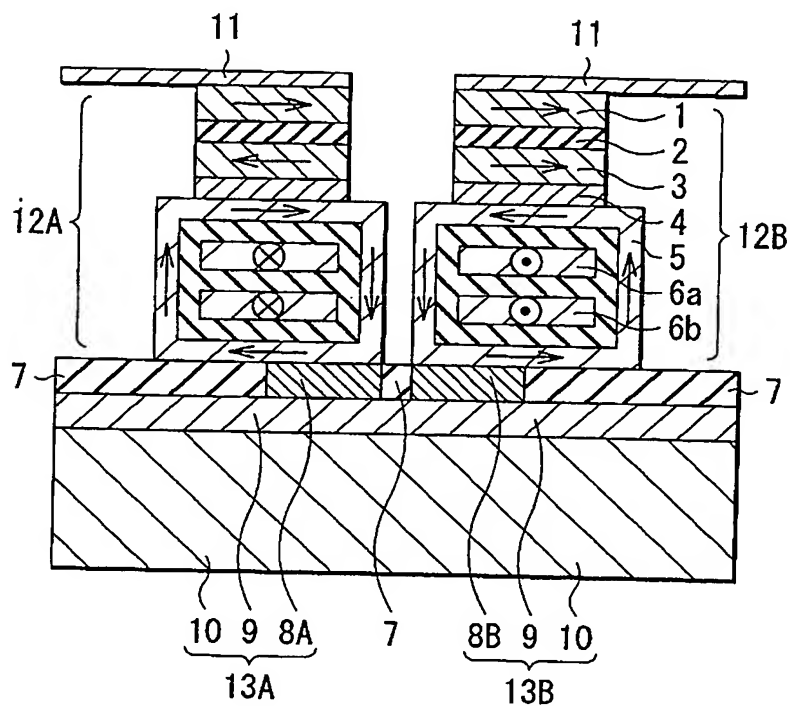
「1」

(B)

【図 1 1】

Fig. 11

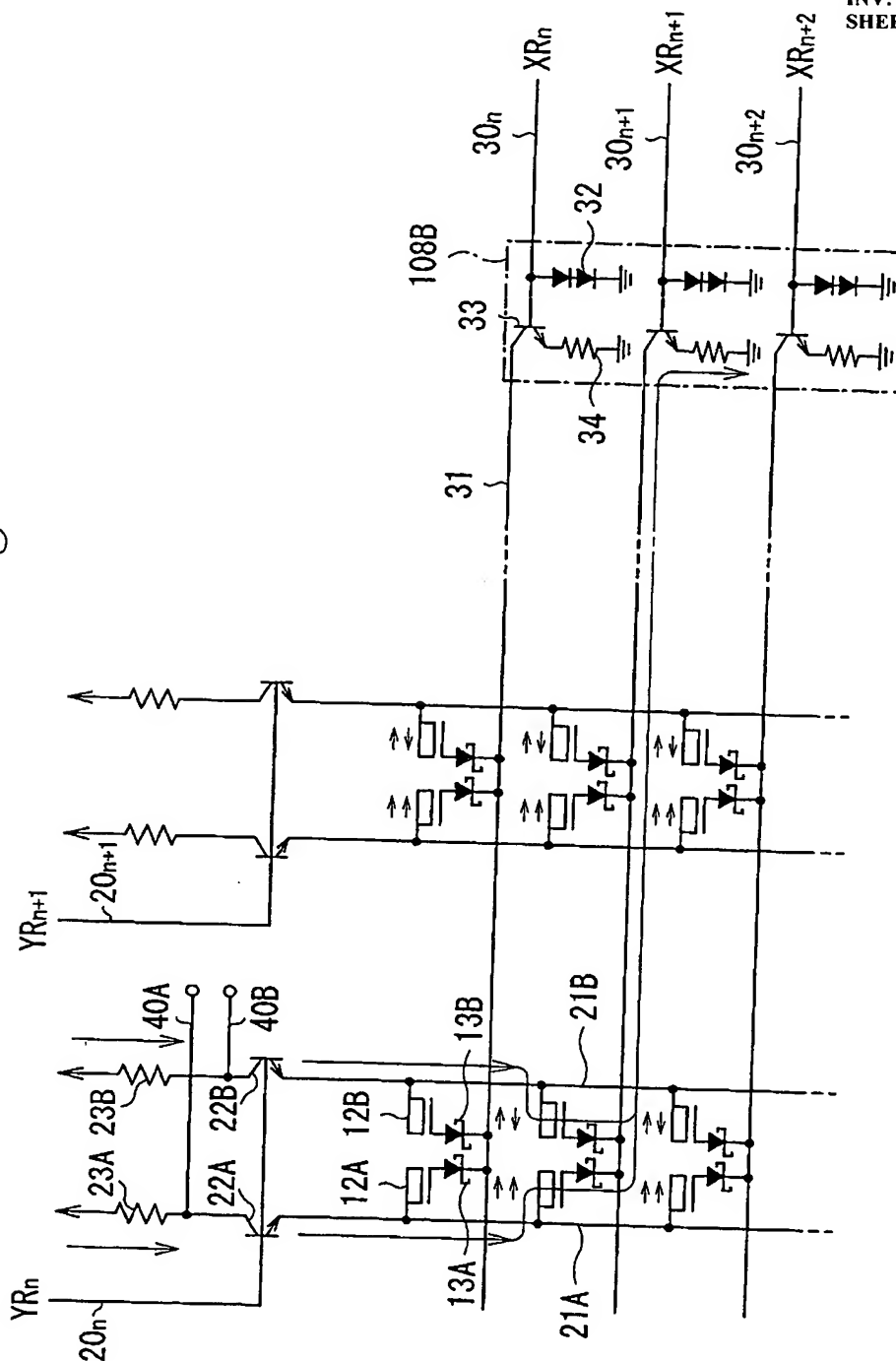
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【図 1 2】

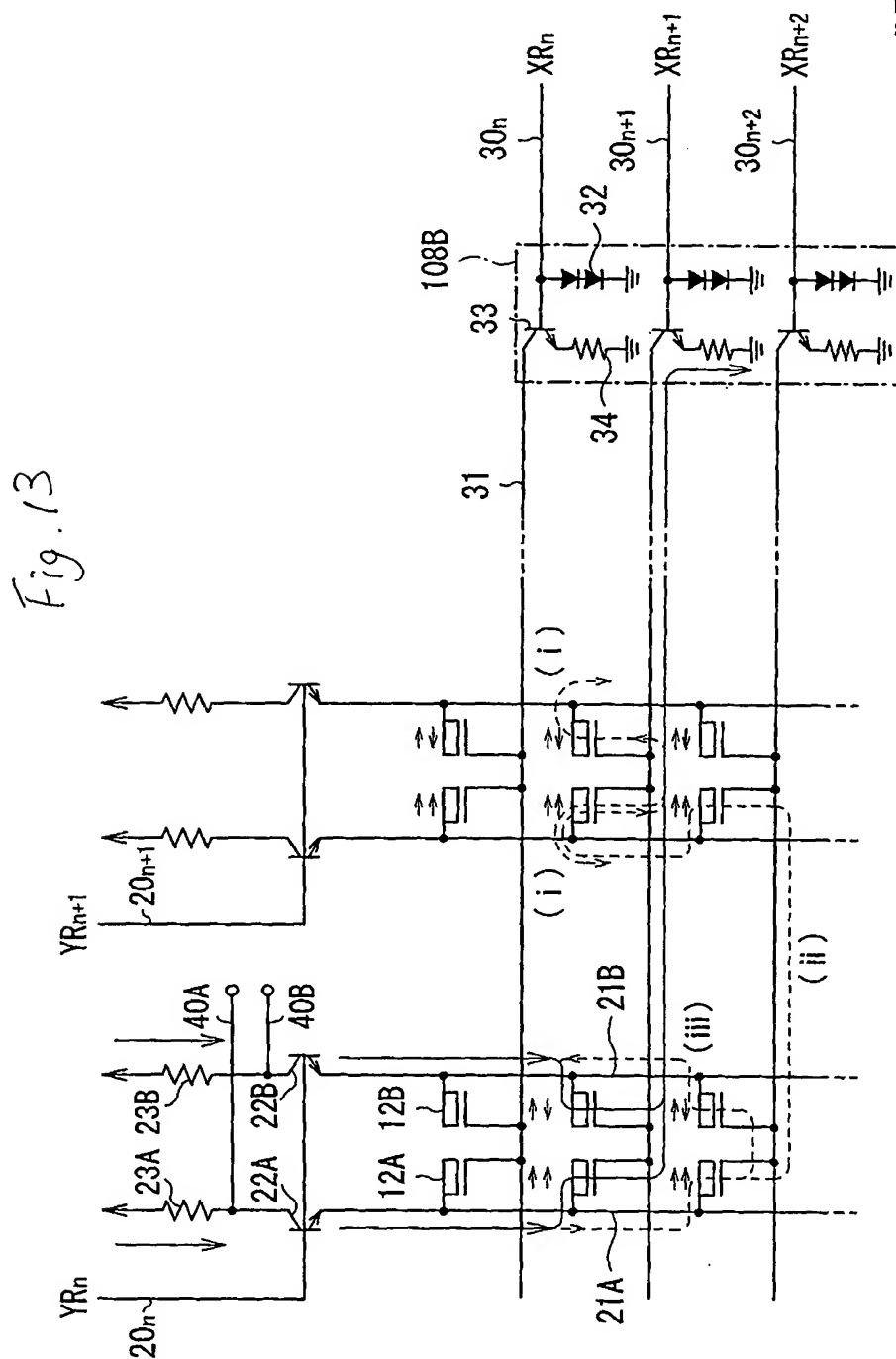
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Fig. 12



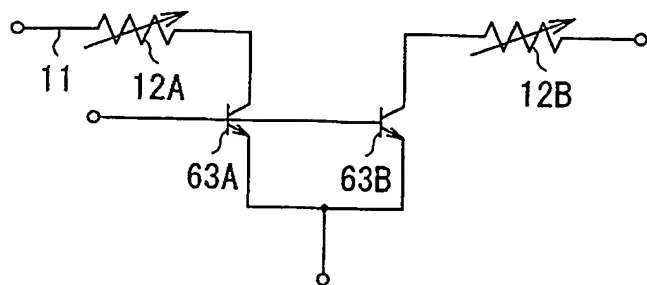
【図 13】

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【図 1 4】

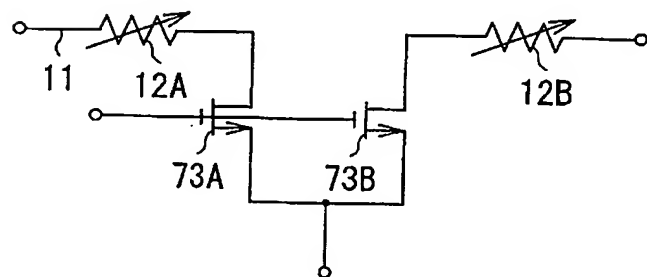
Fig. 14



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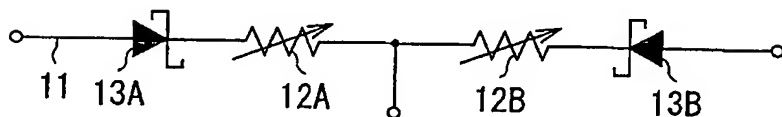
【図 1 5】

Fig. 15



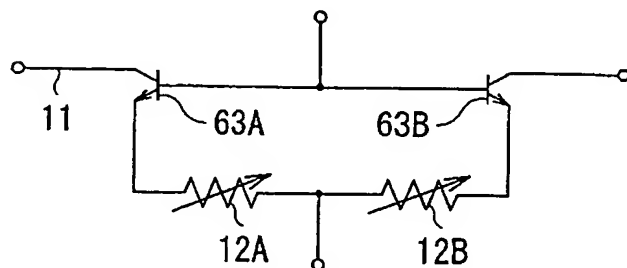
【図 1 6】

Fig. 16



【図 1 7】

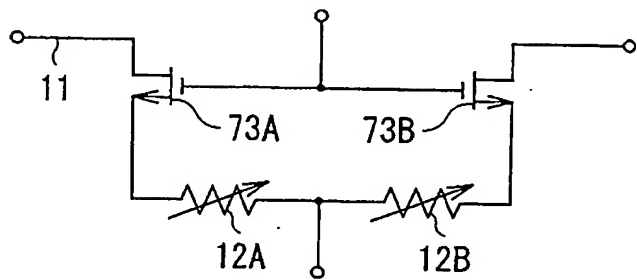
Fig. 17



【図 18】

Fig. 18

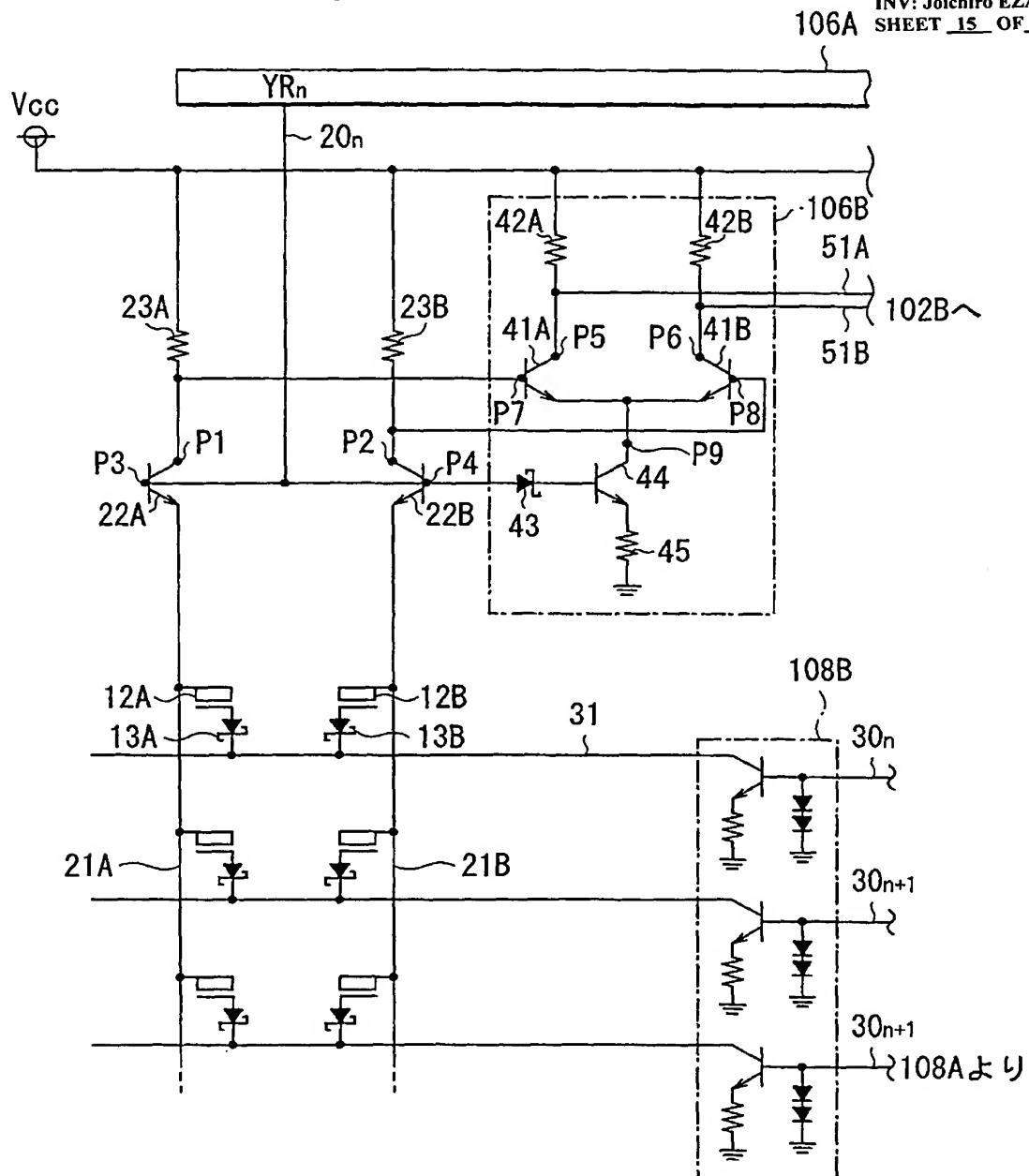
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【図 19】

Fig. 19

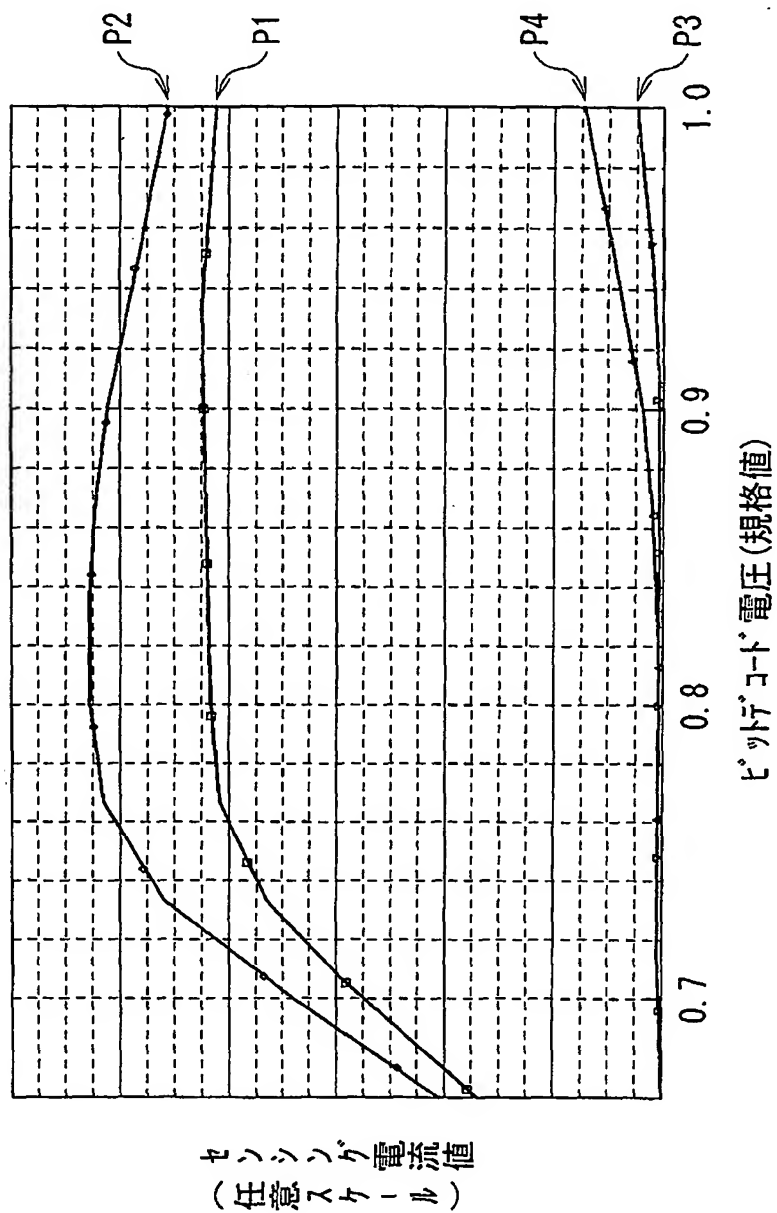
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【図20】

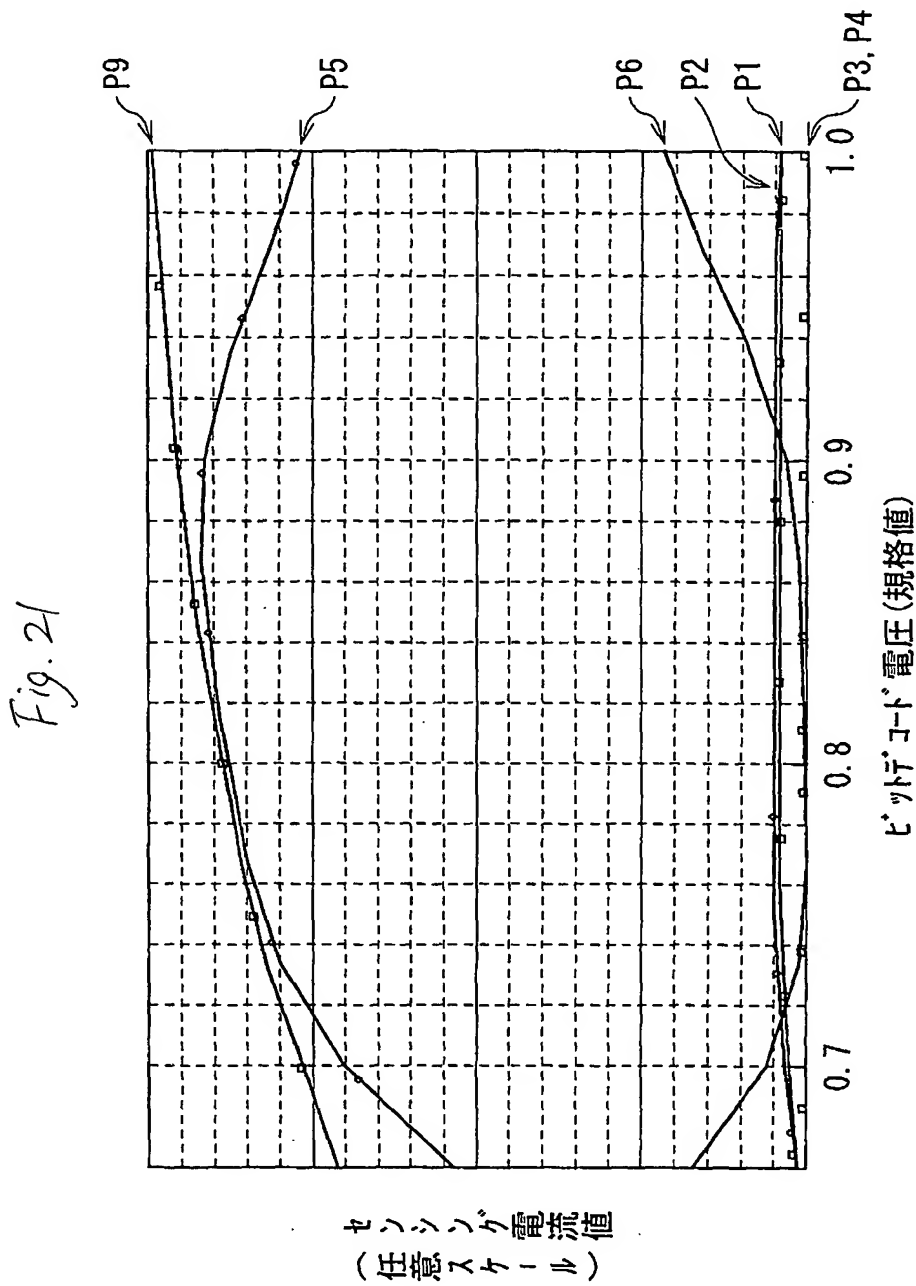
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Fig. 20

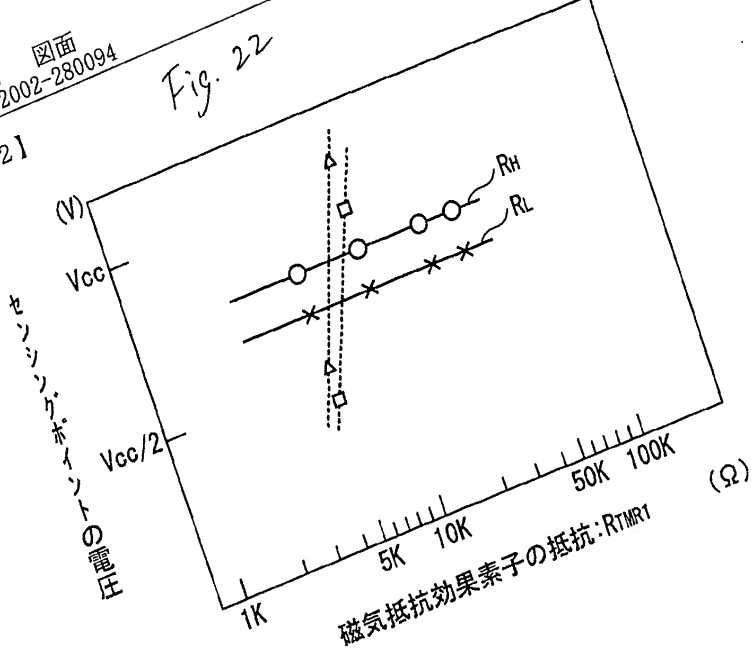


【図 21】

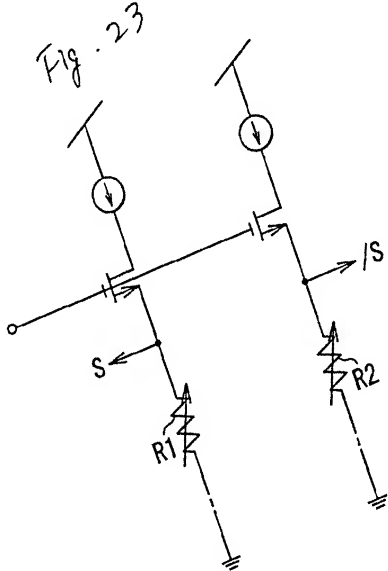
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【図22】



【図23】



【図 24】

Fig. 24

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